Docket No.: 0941-0316P
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Ming-Dou Ker et al.

Application No.: 09/944,171 | Confirmation No.: 009842

Filed: September 4, 2001 | Art Unit: 2815

For: ESD PROTECTION CIRCUIT WITH VERY LOW INPUT CAPACITANCE FOR HIGH-FREQUENCY I/O PORTS | Examiner: J. A. Fenty

BRIEF IN REPLY TO EXAMINER'S ANSWER

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The present Reply Brief is made in response to the Examiner's Answer dated March 22, 2006.

On page 3 of the Examiner's Answer, the Examiner indicated that the Claims Appendix was incorrect because it does not list the withdrawn claims. Applicants point out that this was not an unintentional omission. 37 CFR 41.37(c)(1)(viii) describes the Appendix as containing a copy of the claims involved with the appeal. Since the withdrawn claims are not involved with the appeal, they should not be listed.

In the paragraph bridging pages 9 and 10 of the Examiner's Answer, the Examiner suggests that the presumption is not overcome by a mere showing that it is possible to operate within the disclosure without obtaining the alleged product. Applicants submit that the situation

in Jun et al. does not merely show that it is possible to operate without obtaining the alleged product, but rather that Figure 10 is impossible in view of Figure 9. Column 3, lines 57-59 of Jun et al. specifically point out that the numbered areas of Figure 10 relate the schematic to the cross section in Figure 9. Thus, the reference makes it clear that Figure 10 and Figure 9 are intended to show the same device. Thus, it is not merely showing an alternative, but the specification clearly indicates that the two are equivalent. By showing that the arrangement is not possible in Figure 9, it must follow that the arrangement in Figure 10 is in error.

On page 11 of the Examiner's Answer, the Examiner tries to interpret the term "large area diodes" as meaning that a large current is meant to be passed. Applicants submit that the language of the specification is very clear. It refers to large area diodes and then specifically describes the area involved in terms of the linear dimensions of a side. It is clear that the Patentee is referring to the size of the diodes. Even if this large size can be used for higher voltages, this does not necessarily imply that parallel diodes are meant. The Examiner is attempting to connect a second possible meaning to the clear language of column 3, which is not warranted.

On page 12 of the Examiner's Answer, the Examiner argues that the PN junction lays between region 32 and the substrate. As the Examiner points out, PN junction diodes exist at boundaries. Applicants submit that the clear language of claim 13 indicates that the term "between" means that the junction is formed at the boundary of the two listed elements. The Examiner is attempting to provide the meaning of the word "between" as being arranged between. Applicants submit that this is not the clear meaning of the language of the claim. Thus, the language does not mean that the junction lies somewhere between the two listed regions, but instead means that the junction occurs on the boundary between the two listed regions. Applicants submit that the Examiner's interpretation is not credible and not supported by the specification of the present application.

On page 13 of the Examiner's Answer, the Examiner states that the motivation for inserting a doped area in the first well is found in the Final Rejection. The only motivation given in the Final Rejection at the end of page 3 is "for the purpose of increasing the threshold voltage

of the ESD device." Applicants submit that this is not sufficient motivation. In particular, there is no motivation shown as to why this change would be needed.

On page 14 of the Examiner's Answer, the Examiner refers to a prior art reference, Assaderaghi et al. (U.S. Patent 5,811,857). Applicants submit that the if Examiner is relying on the teaching of this reference, that it should be included in the Statement of the Rejection and that the combination of the teachings should be shown to be obvious.

In addition to the above, Applicants submit that the remaining issues are fully discussed in the Appeal Brief filed originally on March 1, 2004 and filed again on January 4, 2006, to incorporate the additional appendices. In view of this, Applicants have submitted that the Examiner is in error and that the rejection of claims 1-17 should be reversed.

Dated: April 21, 2006

Respectfully submitted,

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